expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints.

15. (Amended) The electronic assembly according to claim 14, wherein the elongation mismatches and the stresses induced thereby in the electronic assembly are reflected in the electronic assembly by at least one of post soldering residual stress, residual plastic deformation in the soldered joints, residual plastic deformation in the substrate, and semiconductor chip warpage.

17. (Amended) An electronic assembly comprising:

a substrate having a first coefficient of thermal expansion;

a semiconductor chip having a second coefficient of thermal expansion which is different than the first coefficient of thermal expansion;

a plurality of soldered joints connecting the semiconductor chip and substrate;

wherein the chip and substrate across the respective soldered joints of the electronic assembly at room temperature have coefficient of thermal expansion difference induced elongation mismatches from soldering; and

wherein the magnitude of the elongation mismatches are less than one-half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints; and

wherein the substrate comprises a plurality of standoff elements upstanding from a surface of the substrate, and wherein the soldered joints connect the semiconductor chip to the tops of respective ones of the standoff elements.

22. (Amended) A semiconductor package comprising:

a package substrate having a first coefficient of thermal expansion of at least 15 ppm/°C, the package substrate having a plurality of contact members;

a semiconductor chip having a coefficient of thermal expansion which is at least 2.7 ppm/°C less than the coefficient of thermal expansion of the package substrate, a front side of the chip having a plurality of solder connections thereon, the semiconductor chip being located on the substrate with the solder connections connected to respective ones of the contact members by soldered joints electrically coupling the semiconductor chip to the package substrate;

wherein the semiconductor chip and package substrate across the respective soldered joints of the semiconductor package at room temperature have coefficient of thermal expansion difference induced elongation mismatches and stresses induced thereby in the semiconductor package from soldering; and

wherein the magnitude of the elongation mismatches and the stresses induced thereby in the semiconductor package are less than one-half that expected based upon cooling the substrate and semiconductor chip from the

solder solidification temperature to room temperature following soldering of the soldered joints.

23. (Amended) The semiconductor package according to claim 22, wherein the elongation mismatches and the stresses induced thereby in the semiconductor package are reflected in the semiconductor package by at least one of post soldering residual stress, residual plastic deformation in the soldered joints, residual plastic deformation in the substrate, and semiconductor chip warpage.

25. (Amended) A semiconductor package comprising:

a package substrate having a first coefficient of thermal expansion of at least 15 ppm/°C, the package substrate having a plurality of contact members;

a semiconductor chip having a coefficient of thermal expansion which is at least 2.7 ppm/°C less than the coefficient of thermal expansion of the package substrate, a front side of the chip having a plurality of solder connections thereon, the semiconductor chip being located on the substrate with the solder connections connected to respective ones of the contact members by soldered joints electrically coupling the semiconductor chip to the package substrate;

wherein the semiconductor chip and package substrate across the respective soldered joints of the semiconductor package at room temperature have coefficient of thermal expansion difference induced elongation mismatches from soldering; and

wherein the magnitude of the elongation mismatches are less than one-half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints; and

wherein the contact members comprise a plurality of standoff elements upstanding from a surface of the substrate, and wherein the soldered joints connect the semiconductor chip to the tops of respective ones of the standoff elements.